IN THE CLAIMS

1. (Currently amended) A field-effect transistor, comprising:
a channel region in a bulk semiconductor substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region;
an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;
a field isolation region laterally adjoining the first source/drain region and extending beneath ~~at least~~ only a portion of the first source/drain region; and
a field isolation region laterally adjoining the second source/drain region and extending beneath ~~at least~~ only a portion of the second source/drain region.

2. (Currently amended) A field-effect transistor, comprising:
a channel region in a bulk semiconductor substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region;
an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;
a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region; and
a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region;
~~The field-effect transistor of claim 1,~~ wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the extensions of epitaxial silicon comprise epitaxial silicon having a conductivity type.

3. (Original) The field-effect transistor of claim 2, wherein the conductivity type of the epitaxial silicon is the second conductivity type.

4. (Original) The field-effect transistor of claim 3, wherein the epitaxial silicon is further doped with germanium.

5. (Currently amended) A field-effect transistor, comprising:

a channel region in a bulk semiconductor substrate;

a first source/drain region on a first side of the channel region and having a polycrystalline portion;

a second source/drain region on a second side of the channel region and having a polycrystalline portion;

first and second extensions of epitaxial silicon formed on the bulk semiconductor substrate, the first and second extensions of epitaxial silicon respectively extending away from the first and second sides of the first channel region, the first extension of epitaxial silicon interposed between the first side of the channel region and the polysilicon portion of the first source/drain region and the second extension of epitaxial silicon interposed between the second side of the channel region and the polysilicon portion of the second source/drain region;

a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region and extending beneath at least a portion of the first extension of epitaxial silicon; and

a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region and extending beneath at least a portion of the second extension of epitaxial silicon.

6. (Currently amended) A field-effect transistor, comprising:

a channel region in a monocrystalline silicon substrate;

a first source/drain region on a first side of the channel region;

a second source/drain region on a second side of the channel region;

epitaxial silicon formed on the monocrystalline silicon substrate so as to extend away from each side of the channel region; and

a gate overlying the channel region;

wherein the monocrystalline silicon substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a

second conductivity type opposite the first conductivity type, and the epitaxial silicon has a conductivity type.

7. (Original) A field-effect transistor, comprising:

a channel region in a monocrystalline silicon substrate;

a first source/drain region on a first side of the channel region and having a polycrystalline portion;

a second source/drain region on a second side of the channel region and having a polycrystalline portion;

epitaxial silicon interposed between the channel region and the polycrystalline portion of each source/drain region; and

a gate overlying the channel region.

8. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath ~~at least~~ only a portion of the first source/drain region; and

a field isolation region laterally adjoining the second source/drain region and extending beneath ~~at least~~ only a portion of the second source/drain region.

9. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region; and

a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region;

~~The memory device of claim 8,~~ wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the extensions of epitaxial silicon comprise epitaxial silicon having a conductivity type.

10. (Original) The memory device of claim 9, wherein the conductivity type of the epitaxial silicon is the second conductivity type.

11. (Original) The memory device of claim 10, wherein the epitaxial silicon is further doped with germanium.

12. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

first and second extensions of epitaxial silicon formed on the bulk semiconductor substrate, the first and second extensions of epitaxial silicon respectively extending away from the first and second sides of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region and extending beneath ~~at least~~ only a portion of the first extension of epitaxial silicon; and

a field isolation region laterally adjoining the second source/drain region and extending beneath at least only a portion of the second source/drain region and extending beneath ~~at least~~ only a portion of the second extension of epitaxial silicon.

13. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor, the first and second source/drain regions each having a polysilicon portion;

wherein the access transistor further comprises:

a channel region in a monocrystalline silicon substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region; and

epitaxial silicon formed on the monocrystalline silicon substrate so as to extend away from each side of the channel region, wherein the epitaxial silicon is interposed between the first side of the channel region and the polysilicon portion of the first source/drain region and between the second side of the channel region and the polysilicon portion of the second source/drain region.

14. (Original) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second polycrystalline source/drain region coupled to the capacitor, each of the first and second source/drain regions having a polycrystalline silicon portion;

wherein the access transistor further comprises:

a channel region in a monocrystalline silicon substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region; and

epitaxial silicon interposed between the channel region and the polycrystalline silicon portion of each source/drain region.

15. (Original) The memory device of claim 14, further comprising a gate overlying the channel region.

16. (Currently amended) A field-effect transistor, comprising:
a channel region in a bulk semiconductor substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region;
an extension of silicon-germanium alloy formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;
a field isolation region laterally adjoining the first source/drain region and extending beneath ~~at least~~ only a portion of the first source/drain region; and
a field isolation region laterally adjoining the second source/drain region and extending beneath ~~at least~~ only a portion of the second source/drain region.

17. (Currently amended) A field-effect transistor, comprising:
a channel region in a bulk semiconductor substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region;
an extension of silicon-germanium alloy formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;
a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region; and
a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region;

~~The field-effect transistor of claim 16,~~ wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the extensions of silicon-germanium alloy comprise silicon-germanium alloy having a conductivity type.

18. (Original) The field-effect transistor of claim 17, wherein the conductivity type of the silicon-germanium alloy is the second conductivity type.

19. (Original) The field-effect transistor of claim 16, wherein the silicon-germanium alloy comprises an epitaxially-grown silicon-germanium alloy.

20. (Original) The field-effect transistor of claim 16, wherein the silicon-germanium alloy comprises approximately 20 at% germanium or more.

21. (Original) The field-effect transistor of claim 20, wherein the silicon-germanium alloy further comprises no more than approximately 50 at% germanium.

22. (Currently amended) A field-effect transistor, comprising:
a channel region in a bulk semiconductor substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region;
first and second extensions of silicon-germanium alloy formed on the bulk semiconductor substrate, the first and second extensions of silicon-germanium alloy respectively extending away from the first and second sides of the channel region;
a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region and extending beneath ~~at least~~ only a portion of the first extension of silicon-germanium alloy; and
a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region and extending beneath ~~at least~~ only a portion of the second extension of silicon-germanium alloy.

23. (Currently amended) A field-effect transistor, comprising:
a channel region in a monocrystalline silicon substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region;
epitaxial silicon-germanium alloy formed on the monocrystalline silicon substrate so as to extend away from each side of the channel region; and
a gate overlying the channel region;
wherein the monocrystalline silicon substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the epitaxial silicon-germanium alloy has a conductivity type.

24. (Original) The field-effect transistor of claim 23, wherein the epitaxial silicon-germanium alloy comprises approximately 20 at% germanium or more.

25. (Original) The field-effect transistor of claim 24, wherein the epitaxial silicon-germanium alloy further comprises no more than approximately 50 at% germanium.

26. (Original) A field-effect transistor, comprising:
a channel region in a monocrystalline silicon substrate;
a first source/drain region on a first side of the channel region and having a polycrystalline portion;
a second polycrystalline silicon source/drain region on a second side of the channel region and having a polycrystalline portion;
epitaxial silicon-germanium alloy interposed between the channel region and the polycrystalline portion of each source/drain region; and
a gate overlying the channel region.

27. (Original) The field-effect transistor of claim 26, wherein the epitaxial silicon-germanium alloy comprises between approximately 20-50 at% germanium.

28. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

an extension of epitaxial silicon-germanium alloy formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath ~~at least~~ only a portion of the first source/drain region; and

a field isolation region laterally adjoining the second source/drain region and extending beneath ~~at least~~ only a portion of the second source/drain region.

29. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

<u>a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;</u>

<u>an extension of epitaxial silicon-germanium alloy formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;</u>

<u>a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region; and</u>

<u>a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region;</u>

~~The memory device of claim 28,~~ wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the extensions of silicon-germanium alloy comprise silicon-germanium alloy having a conductivity type.

30. (Original) The memory device of claim 29, wherein the conductivity type of the silicon-germanium alloy is the second conductivity type.

31. (Original) The memory device of claim 28, wherein the silicon-germanium alloy comprises an epitaxially-grown silicon-germanium alloy.

32. (Original) The memory device of claim 28, wherein the silicon-germanium alloy comprises approximately 20 at% germanium or more.

33. (Original) The memory device of claim 32, wherein the silicon-germanium alloy further comprises no more than approximately 50 at% germanium.

34. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

first and second extensions of epitaxial silicon-germanium alloy formed on the bulk semiconductor substrate, the first and second extensions of epitaxial silicon-germanium alloy respectively extending away from the first and second sides of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region and extending beneath ~~at least~~ <u>only</u> a portion of the first extension of epitaxial silicon-germanium alloy; and

a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region and extending beneath ~~at least~~ <u>only</u> a portion of the second extension of epitaxial silicon-germanium alloy.

35. (Currently amended) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a monocrystalline silicon substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region; and

epitaxial silicon-germanium alloy formed on the monocrystalline silicon substrate so as to extend away from each side of the channel region;

wherein the monocrystalline silicon substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the epitaxial silicon-germanium alloy has a conductivity type.

36. (Original) A memory device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first polycrystalline silicon source/drain region coupled to a bit line and a second polycrystalline source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a monocrystalline silicon substrate with the first polycrystalline silicon source/drain region on a first side of the channel region and the second polycrystalline silicon source/drain region on a second side of the channel region; and

epitaxial silicon-germanium alloy formed on the monocrystalline silicon substrate so as to extend away from each side of the channel region.

37. (Currently amended) An electronic system comprising:

a processor;

a memory device coupled to the processor, the memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath ~~at least~~ <u>only</u> a portion of the first source/drain region; and

a field isolation region laterally adjoining the second source/drain region and extending beneath ~~at least~~ <u>only</u> a portion of the second source/drain region.

38. (Currently amended) <u>An electronic system comprising:</u>

<u>a processor;</u>

<u>a memory device coupled to the processor, the memory device comprising:</u>

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

an extension of epitaxial silicon formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath at least a portion of the first source/drain region; and

a field isolation region laterally adjoining the second source/drain region and extending beneath at least a portion of the second source/drain region;

~~The electronic system of claim 37,~~ wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the extensions of epitaxial silicon comprise epitaxial silicon having a conductivity type.

39. (Original) The electronic system of claim 38, wherein the conductivity type of the epitaxial silicon is the second conductivity type.

40. (Original) The electronic system of claim 39, wherein the epitaxial silicon is further doped with germanium.

41. (Currently amended) An electronic system comprising:

a processor;

a memory device coupled to the processor, the memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region;

an extension of epitaxial silicon-germanium alloy formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;

a field isolation region laterally adjoining the first source/drain region and extending beneath ~~at least~~ <u>only</u> a portion of the first source/drain region; and

a field isolation region laterally adjoining the second source/drain region and extending beneath ~~at least~~ <u>only</u> a portion of the second source/drain region.

42. (Original) The electronic system of claim 41, wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first

conductivity type, and the extensions of silicon-germanium alloy comprise silicon-germanium alloy having a conductivity type.

43. (Original) The electronic system of claim 42, wherein the conductivity type of the silicon-germanium alloy is the second conductivity type.

44. (Original) The electronic system of claim 41, wherein the silicon-germanium alloy comprises an epitaxially-grown silicon-germanium alloy.

45. (Original) The electronic system of claim 41, wherein the silicon-germanium alloy comprises approximately 20 at% germanium or more.

46. (Original) The electronic system of claim 45, wherein the silicon-germanium alloy further comprises no more than approximately 50 at% germanium.

47. (Currently amended) A field-effect transistor, comprising:

a channel region in a bulk semiconductor substrate;

a first source/drain region on a first side of the channel region and having a polysilicon portion;

a second source/drain region on a second side of the channel region and having a polysilicon portion; and

an extension of epitaxial monocrystalline material formed on the bulk semiconductor substrate so as to extend away from each side of the channel region, wherein a first extension of epitaxial monocrystalline material is interposed between the first side of the channel region and the polysilicon portion of the first source/drain region and a second extension of epitaxial monocrystalline material is interposed between the second side of the channel region and the polysilicon portion of the second source/drain region.

48. (Original) The field-effect transistor of claim 47, wherein the extensions of epitaxial monocrystalline material are of epitaxial silicon.

49. (Original) The field-effect transistor of claim 48, wherein the extensions of epitaxial silicon are of doped epitaxial silicon.

50. (Original) The field-effect transistor of claim 49, wherein the doped epitaxial silicon is doped with germanium.

51. (Original) The field-effect transistor of claim 47, wherein the extensions of monocrystalline material are an epitaxially grown silicon-germanium alloy.

52. (Original) The field-effect transistor of claim 51, wherein the silicon-germanium alloy comprises approximately 20 at% germanium or more.

53. (Original) The field-effect transistor of claim 52, wherein the silicon-germanium alloy further comprises no more than approximately 50 at% germanium.

54. (Currently amended) A field-effect transistor, comprising:
a channel region in a bulk semiconductor substrate;
a first source/drain region on a first side of the channel region;
a second source/drain region on a second side of the channel region; and
an extension of epitaxial monocrystalline material formed on the bulk semiconductor substrate so as to extend away from each side of the channel region;
~~The field-effect transistor of claim 47,~~ wherein the bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type, the source/drain regions comprise polysilicon having a second conductivity type opposite the first conductivity type, and the extensions of epitaxial monocrystalline material comprise epitaxial silicon having a conductivity type.

55. (Original) The field-effect transistor of claim 54, wherein the conductivity type of the epitaxial silicon is the second conductivity type.

56. (Currently amended) A memory device, comprising:
a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor, the first and second source/drain regions each comprising a polysilicon portion;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and the second source/drain region on a second side of the channel region; and

an ~~extension of~~ epitaxial monocrystalline material formed on the bulk semiconductor substrate ~~so as to extend away from each side of~~ and interposed between the channel region and the polysilicon portions of the first and second source/drain regions.

57. (Currently amended) An electronic system comprising:

a processor;

a memory device coupled to the processor, the memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells, wherein each memory cell comprises:

a capacitor; and

an access transistor having a gate coupled to a word line, a first source/drain region coupled to a bit line and a second source/drain region coupled to the capacitor, the first and second source/drain regions each comprising a polysilicon portion;

wherein the access transistor further comprises:

a channel region in a bulk semiconductor substrate with the first source/drain region on a first side of the channel region and

the second source/drain region on a second side of the channel region; and

an ~~extension of~~ epitaxial monocrystalline material formed on the bulk semiconductor substrate ~~so as to extend away from each side of~~ and interposed between the channel region and the polysilicon portions of the first and second source/drain regions.